FIGS. **1–10** are cross sectional elevation views of the first preferred embodiment and the steps of the preferred embodiment fabrication method.

FIGS. **11–22** are cross sectional elevation views of the second preferred embodiment and the steps of the second preferred embodiment fabrication method.

DETAILED DESCRIPTION OF THE DRAWINGS

The first preferred embodiment method for fabricating bipolar transistors includes the following steps as illustrated in cross sectional elevation views in FIGS. **1–10**.

In FIG. **1**, a substrate material **30** is composed of a semiconductor material, such as GaAs. A GaAs subcollector layer **31** is grown by, for example molecular beam epitaxy, with n-type doping of 3×10^{18} cm^{-3} Si and thickness of 500 nm. A collector layer is grown consisting of 500 nm doped n-type at 3×10^{16} cm^{-3}. The collector layer is composed of AlGaAs layer **32** and an optional GaAs layer **33**. A base epilayer **34** of GaAs is deposited on to the collector **32** at a thickness of 50 nm and doped with C at a concentration of 5×10^{19} cm^{-3}. Emitter epilayer **36** of n-type AlGaAs is deposited onto base layer **34** at a thickness of 50 nm and doping of 2×10^{17} cm^{-3}. A GaAs emitter cap layer **37** is then deposited with thickness of 300 nm and doping of 5×10^{18}, cm^{-3}.

In FIG. **2**, photoresist **39** is applied and patterned by lithography. Emitter contact metal **38** is then evaporated, consisting of 50 nm AuGe, 14 nm Ni, and 200 nm Au. The excess metal **41** on top of the photoresist **39** is then lifted off by dissolving the photoresist in acetone.

In FIG. **3**, the emitter cap **37** and the emitter layer **36** are etched using the emitter contact **38** as a mask.

In FIG. **4**, the base contacts **40** are evaporated onto the base layer **34** using a lift-off process. The base contact metal consists of 50 nm Ti, 25 nm Pt, and 200 nm Au.

In FIG. **5**, a layer of photoresist **43** is deposited and patterned over the emitter and portions of the base contacts.

In FIG. **6**, the base layer **34** and the collector layers **32** and **33** are etched using the base contact **40** and photoresist **43** as a mask.

In FIG. **7**, a layer of silicon nitride is deposited over the base contact **40**, the emitter **36** and the emitter contact **38** to protect the AlGaAs in the emitter.

In FIG. **8**, a timed selective etch is used to etch the AlGaAs of the collector layer **32** and produce an undercut **45** beneath the base layer **34**.

In FIG. **9**, the layer of silicon nitride is removed.

In FIG. **10**, 50 nm thick AuGe emitter ohmic contact metal, followed by 14 nm Ni and 200 nm Au layers are evaporated onto the subcollector **31** using a lift-off process to make the collector contact **44**. The contacts are then alloyed by heating to 430 degrees Celsius for 1 minute.

The second preferred embodiment method for fabricating high power heterojunction bipolar transistors (HBTs) includes the following steps as illustrated in cross sectional elevation views in FIGS. **11–22**. In the second preferred embodiment, ion implantation is used to convert the upper portion of the collector in the extrinsic base region to the doping type of the base to reduce the extrinsic base resistance. The base-collector capacitance is not affected by this implant, because the implanted material is separated from the collector by the air gap produced by the undercut etch.

The fabrication of the second preferred embodiment is similar to that of the first embodiment, except that after the etch to the base and before forming the base contacts, dopant is introduced to the extrinsic base region by diffusion or ion implantation. The emitter metal or photoresist may be used to protect the active device region under the emitter contact.

In FIG. **11**, a substrate material **30** is composed of a semiconductor material, such as GaAs. A GaAs subcollector layer **31** is grown by, for example molecular beam epitaxy, with n-type doping of 3×10^{18} cm^{-3} Si and thickness of 500 nm. A collector layer is grown consisting of 500 nm doped n-type at 3×10^{16} cm^{-3}. The collector layer is composed of AlGaAs layer **32** and an optional GaAs layer **33**. A base epilayer **34** of GaAs is deposited on to the collector **32** at a thickness of 50 nm and doped with C at a concentration of 5×10^{19} cm^{-3}. Emitter epilayer **36** of n-type AlGaAs is deposited onto base layer **34** at a thickness of 50 nm and doping of 2×10^{17} cm^{-3}. A GaAs emitter cap layer **37** is then deposited with thickness of 300 nm and doping of 5×10^{18} cm^{-3}.

In FIG. **12**, photoresist **39** is applied and patterned by lithography. Emitter contact metal **38** is then deposited, consisting of a refractory metal, such as 200 nm WSi. The excess metal **41** on top of the photoresist **39** is then lifted off by dissolving the photoresist in acetone.

In FIG. **13**, the emitter cap **37** and the emitter layer **36** are etched using the emitter contact **38** as a mask.

In FIG. **14**, 40 nm of silicon nitride **41** is deposited on top of the base layer **34**. The structure is then ion implanted (for example, Be at 60 keV to a dose of 1×10^{14} cm^{-2}) to convert the collector layer **33** immediately under the base layer in the extrinsic base region. The emitter acts as a mask. The structure is then annealed at 800 C. for 30 seconds to activate the implant.

In FIG. **15**, the silicon nitride is then removed to leave a ion-implanted portion **47** of the collector layer. The implanted region may extend through the GaAs collector layer **33** and partially into the AlGaAs collector layer **32**.

In FIG. **16**, the base contacts **40** are evaporated onto the base layer **34** using a lift-off process. The base contact metal consists of 50 nm Ti, 25 nm Pt, and 200 nm Au.

In FIG. **17**, a layer of photoresist **43** is deposited and patterned over the emitter and portions of the base contacts.

In FIG. **18**, the base layer **34** and the collector layers **32** and **33** are etched using the base contact **40** and photoresist **43** as a mask.

In FIG. **19**, a layer of silicon nitride is deposited over the base contact **40**, the emitter **36** and the emitter contact **38** to protect the AlGaAs in the emitter.

In FIG. **20**, a timed selective etch is used to etch the collector layer **32** and produce an undercut **45** beneath the base layer **34**. The selective etch may be either dopant selective or material selective.

In FIG. **21**, the layer of silicon nitride is removed.

In FIG. **22**, 50 nm thick AuGe emitter ohmic contact metal, followed by 14 nm Ni and 200 nm Au layers are evaporated onto the subcollector **31** using a lift-off process to make the collector contact **44**. The contacts are then alloyed by heating to 430 degrees Celsius for 1 minute.

What is claimed is:

1. A method for fabricating a bipolar transistor, comprising the steps of:

a. forming an emitter contact on a material structure including:

i. a collector layer over a subcollector layer;

ii. a base layer formed over said collector layer;

iii. an emitter layer formed over said base layer;